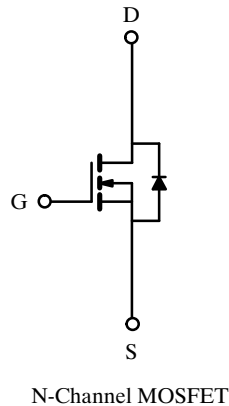
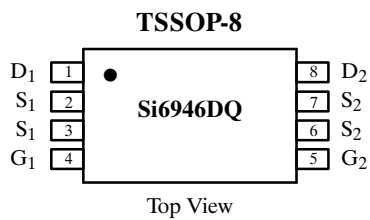


Dual N-Channel Enhancement-Mode MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.080 @ V _{GS} = 4.5 V	2.8
	0.110 @ V _{GS} = 2.5 V	2.1



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±8	
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	A
		T _A = 70°C	
Pulsed Drain Current	I _{DM}	20	A
Continuous Source Current (Diode Conduction) ^a	I _S	1.0	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	W
		T _A = 70°C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1810.

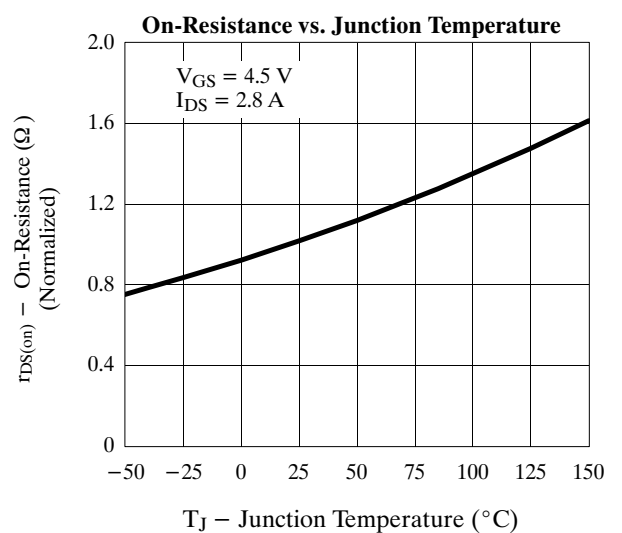
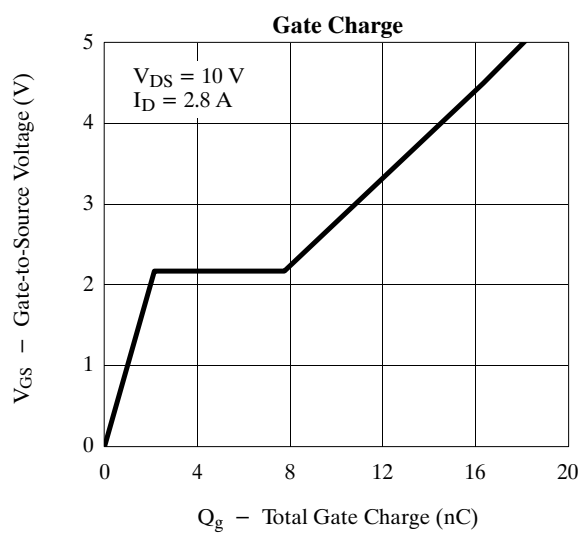
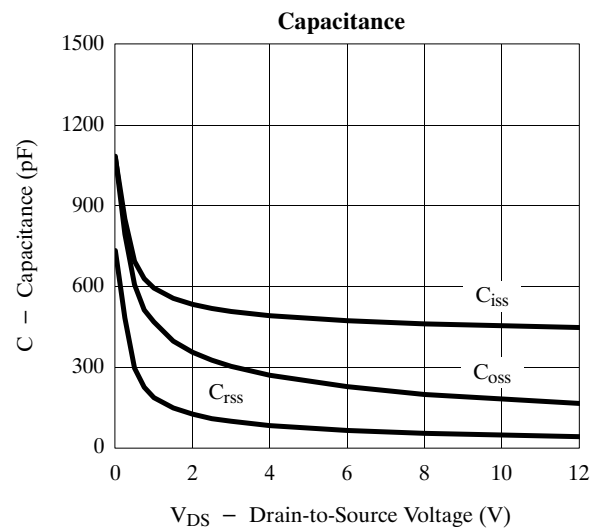
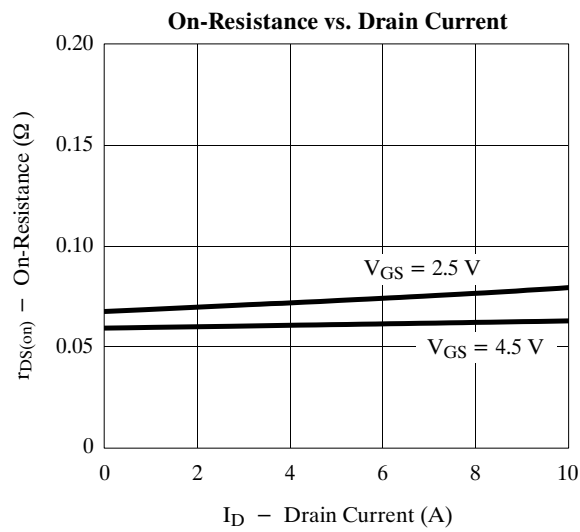
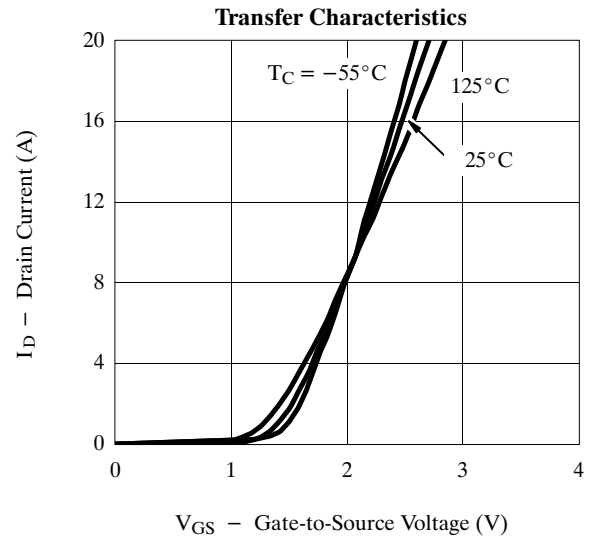
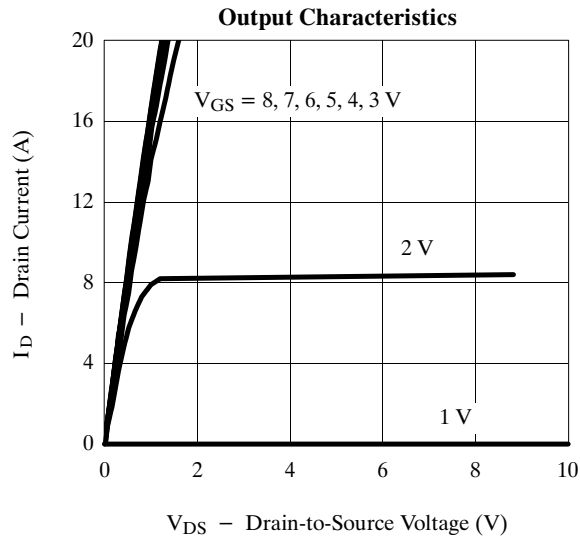
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	± 10			A
On-State Drain Current ^a		$V_{DS} = 5\ \text{V}, V_{GS} = 2.5\ \text{V}$	± 4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 2.8\ \text{A}$			0.080	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 2.1\ \text{A}$			0.110	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 2.8\ \text{A}$				S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.0\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 2.8\ \text{A}$		16	40	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		37	60	ns
Rise Time	t_r			66	100	
Turn-Off Delay Time	$t_{d(off)}$			56	100	
Fall Time	t_f			57	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.0\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		26	70	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

